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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|-------------------------|---------------------|------------------|
| 10/520,441 | 09/01/2005 | Katarzyna Leijten-Nowak | NL 020632 | 5614 |

7590 03/05/2007
Philips Electronics North America Corporation
Corporate Patent Counsel
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| EXAMINER |
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TAN, VIBOL

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| ART UNIT | PAPER NUMBER |
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2819

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|--|------------|---------------|
| 2 MONTHS | 03/05/2007 | PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Art Unit: 2819

1. This application is in condition for allowance except for the following formal matters:

Fig. 1 must be labeled as PRIOR ART.

Suitable descriptive legends may be used, where necessary for understanding of the drawing, subject to approval by the office. They should contain as few words as possible. See MPEP 608.02; 37 CFR 184(o).

For example in Fig. 2, suitable descriptive legends may be used to identify each element or component in order to help understanding the drawing.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

Allowable Subject Matter

2. The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach the programmable logic units being coupled to successive positions along the carry chain at least in the multi-bit operand mode, so as to process carry signals from the carry chain, the output circuit selecting an output signal from the programmable logic units under control of further input signals in the random logic mode and passing outputs from the programmable logic units in parallel in the multi-bit operand mode, as required by claim

1.

3. Claims 1-13 are in condition for allowance.


Art Unit: 2819

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


VIBOL TAN
PRIMARY EXAMINER